Replacement sheet

DUT, XACTOR

1
CPU

FBUS

DUT,
DUT_CORE,
XACTOR

12
BRIDGE

2
MEMORY

DUT

DUT

3
I/O

F I G U R E   1 -- Prior art --

E

D

C++

C_Port$_0$

B_Port$_0$

C++

A_Port$_0$

HDL

C_Port$_n$

B_Port$_n$

C++

A_Port$_n$

HDL

Port$_0$ ...   Port$_n$

INTERFACE

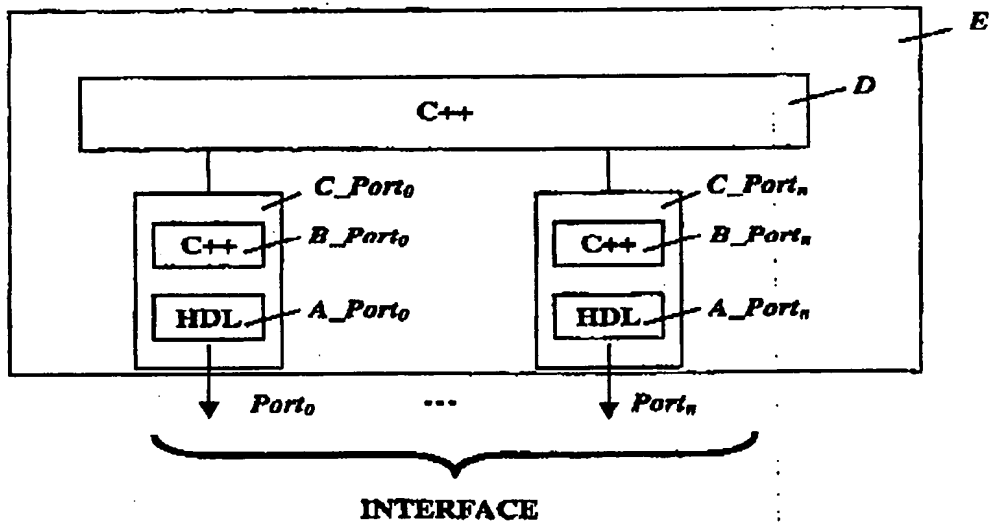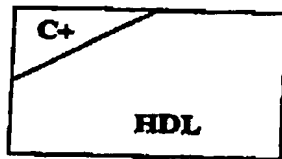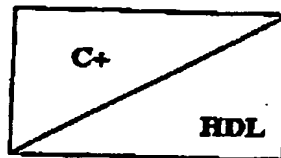**Figure 5 : Generic structure of a C++ Composite Model** -- Prior art --
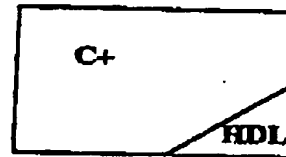
Replacement sheet

HDL Modeling   General case   C++ Modeling

Fig. 3a -- Prior art --   **Fig. 3b** -- Prior art --   **Fig. 3c** -- Prior art --
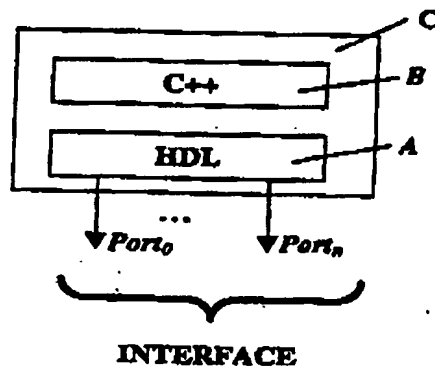

INTERFACE

Figure 4 : Generic Structure of an Elementary Model

TCRC	%InstNameModuleMap
TCRC	%SysConnectMap
TCRC	%SysSpecMap
TCRC	%SysWrapMap
TCRC	%SysPinConst
TCRC	%Activity_TypeMap
TCRC	%PortProbeMap
TRCOH	%HwfConnectivityMap
TRCOH	%HwifAlternateMap
TFMT	%moduleToCppClassMap
TFMT	%classCppProtoMap

Figure 6